**Computer Organization**

**(Theory)**

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| **Subject Code:** | 18CS35/18IS35 | **Credits:** | 3 |
| **Course Type:** | PC3 | **CIE Marks:** | 50 marks |
| **Hours/week: L – T – P** | 3– 0 – 0 | **SEE Marks:** | 50 marks |
| **Total Hours:** | 40 | **SEE Duration:** | 3 Hours for 100 Marks |

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| **Course learning objectives** | |
| 1. | To understand the operation of CPUs including I/O, Processor, Memory systems, Bus and Computer Arithmetic. |
| 2. | To understand the different ways of communicating with I/O devices and to introduce the hierarchical memory system including cache memories. |
| 3. | To understand the implementation of different computer arithmetic algorithms for various arithmetic operations. |
| 4. | To study the internal functional units of processor and understand the generation of internal functions to execute instructions, pipelining and embedded systems. |

**Prerequisites: Digital Electronics.**

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| **Unit – I** | | **08 Hours** | |
| **Basic Structure of Computers:** Functional Units, Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement, Machine Instructions and Programs: Numbers, Arithmetic Operations and Characters, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing. Addressing Modes.  **Self learning topics:** Computer Types, Historical Perspective | | | |
| **Unit – II** | **08 Hours** | |  |
| **Input/Output Organization:** Accessing I/O Devices, Program controlled I/O, Memory mapped I/O, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access, Bus Arbitration Techniques: Centralized & Distributed, Buses : Synchronous & Asynchronous | | |  |

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| **Unit – III** | **08 Hours** |
| **Memory System**: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories–Mapping Functions: Direct mapping, Associative Mapping, Set-associative Mapping. | |

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| **Unit – IV** | **08 Hours** |
| **Arithmetic:** Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers, Signed Operand Multiplication, Fast Multiplication, Integer Division.   |  | | --- | | Application of the algorithms for arithmetic operations. | | **Self learning topics:** Floating-point Numbers and Operations | | |

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| **Unit – V** | **08 Hours** |
| |  | | --- | | **Basic Processing Unit:**  Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control. | | **Self learning topics:** Embedded Systems | | |

**Text Books**

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002 and onwards. Chapter 1, 2, 4, 5, 6, 7 & 9

**Reference Books**

1. Computer Architecture, A Quantitative Approach – John L. Hennessey and David A. Patterson: 5th Edition, Elsevier and onwards.
2. William Stallings: Computer Organization & Architecture, 8th Edition, PHI, 2006 and onwards.

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| **Course Outcome (COs)** | | | |
| At the end of the course, the student will be able to | | **Bloom’s Level** | |
| 1. | **Identify** the functional units of the processor and the factors affecting the performance of a computer | L1 | |
| 2. | **Explain** the addressing modes and instructions sets. | L2 | |
| 3. | **Discuss** the algorithms for computer arithmetic operations and learn the working of those algorithms for arithmetic operations | L3 | |
| 4. | **Infer** the internal functional units of processor and generate sequence of signals to execute different instructions | L4 | |
| **Program Outcome of this course (POs)** | | | **PO No.** |
| 1. | **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems. | | **1** |
| 2. | **Conduct investigation of complex problems:** Use research based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusion. | | **4** |
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| **Course delivery methods** | | **Assessment methods** | |
| 1. | Chalk and board | 1. | Internal assessment |
| 2. | PPT | 2. | Assignment |
| 3. | Video lectures | 3. | Quiz |
|  |  | 4. | Seminar / project |

**Scheme of Continuous Internal Evaluation (CIE):**

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| Components | | | Addition of two IA tests. | Average of two assignments | Quiz/Seminar/Course Project | Total  Marks |  |  |
| Maximum Marks: 50 | | | 15+15=30 | 10 | 10 | 50 |  |  |
| * Writing two IA test is compulsory. * **Minimum marks required to qualify for SEE :20 out of 50** | | | | | | |  |  |
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| **Scheme of Semester End Examination (SEE):** | | | | | | | | |
| 1. | | It will be conducted for 100 marks of 3 hours duration. It will be reduced to 50 marks for the calculation of SGPA and CGPA. | | | | | | |
| 2. | | **Minimum marks required in SEE to pass:40** | | | | | | |
| 3. | | Question paper contains 10 questions each carrying 20 marks. Students have to answer FIVE full questions. | | | | | | |